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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,399	04/14/2005	Franciscus Johannes Klosters	NL02 1019 US	8141

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

NOTIFICATION DATE	DELIVERY MODE
10/10/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/531,399	KLOSTERS ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/14/2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are currently pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 7/23/2007.

Withdrawn objections and rejections

3. The objections to claims 1, 2, 4, 6, 7, and 9 have been withdrawn due to amendment.

4. The 35 U.S.C. 112 second paragraph rejections for claims 1-8 have been withdrawn due to amendment.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of claims 1-9 must be shown or the feature(s) canceled from the claim(s). The limitations for claims 1-9 aren't shown in the drawings by the empty boxes present in figures 1, 3, and 5-6. The objection will be withdrawn when these boxes are filled with their corresponding labels from the specification. No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Maintained Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, and 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hongbin Hao et al. (U.S. 6,163,586, hereinafter Hao).

8. As per claim 1:

Hao disclosed a data processing apparatus, the apparatus comprising:

An input port for receiving a communication signal that contains temporally successive bits (Hao: Figures 3-4 element 14, column 3 lines 38-41 and column 6 lines 51-63)(Temporally successive bits is interpreted as successive bits received over time. Input element 14 receives serial bits as shown in figure 3.);

An output port for outputting a data word formed from respective ones of the temporally successive bits (Hao: Figures 3-4 element 16, column 3 lines 38-41 and column 7 lines 11-14)(Output element 16 receives the data word and echo's it through.);

A programmable processor circuit coupled to the input port, the processor executing a plurality of series of programmed instructions in support of said receiving or said outputting (Hao: Figures 4-5 element 20)(Element 20 is coupled to element 14 and is programmable since it's originally programmed prior to fabrication. An instruction in its broadest sense is a command and/or explanation of how to perform a given task. In this definition, instructions are present within the state diagram of figure 5 to perform

comparisons to detect certain given characters at elements 58, 68, 70, and 80. These comparisons make up the series of programmed instructions.), each at a time of reception of a respective ones of the temporally successive bits, the processor circuit suspending operation each time after executing a respective one of the series of instructions (Hao: Figures 3 and 5 elements 56 and 64, column 7 lines 51-60)(The processor is suspended between start bits as shown in figure 3 and elements 56 and 64.);

A synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective ones of the temporally successive bits (Hao: Figures 4-5 elements 32, 56, and 64, column 7 lines 11-27)(Element 32 performs the determining steps of elements 56 and 64, which determines if a start bit is within a legal window. If a start bit is within a legal window, this triggers the state diagram to continue to elements such as 58, 68, 70, and 80 that perform a series of instructions.), and, except for a last one of the series, prior to reception of one or more later bits that contribute to the data word (Hao: Figure 4 elements 14, 20, 22, and 32)(It's inherent that for a last bit of the series, it must be received via element 14 prior to having any actions performed on it by elements 20, 22, and 32.).

9. As per claim 2:

Hao disclosed a data processing apparatus according to claim 1, wherein the programmable processor (element 12 figure 4) is programmed to compute cumulative information [the state in the flow diagram of figure 5], corresponding to a function of a

combination of the bits from which the data word is formed [the determination of the character received from the received bits (column 7 line 60 to column 8 line 17)], each series of instructions being programmed to add a contribution (the new state in the flow of figure 5) to the cumulative information (the old state in the flow of figure 5) of the respective ones of the temporally successive bits at the time of reception of which the series is executed [the changing state in the flow depending on the series of bit received previously (column 7 line 60 to column 8 line 17)].

10. As per claim 4:

Hao disclosed a data processing apparatus according to claim 1, wherein the processor circuit is constructed sequence instruction execution [the operation executed by the circuit depends on the state of the flow in figure 5]; the operation is inherently triggered by some signals (using handshake signals), execution of each of the instruction in the series being triggered by a respective request signal [each operation is triggered by receiving a new data bit through input port (column 7 line 60 to column 8 line 17)], execution of each instruction of the series, except for a last instruction in each series, generating the request signal for a next one of the instructions in the series [each operation trigger a next step or repeat the same operation (active wait) (figure 5)], the synchronization circuit being coupled to apply the request signals for the initial one of the instructions in the series [the synchronization circuit receives the signal coming into the input port (column 6 lines 62-66) and the circuit trigger the operation in the flow].

11. As per claim 5:

Hao disclosed a data processing apparatus according to claim 1, wherein the synchronization circuit (element 32, 20 figure 4) is arranged to adapt a frequency of triggering the execution of the series of instructions under control of a timing of transitions in the communication signal [the incoming signal is analysis to determine the value of M by the baud rate determination means and the value of M is sent to the synchronization circuit (column 7 lines 13-26) through the usage of value M (BT, BT=32M column 7 lines 57-60) the synchronization circuit is adapt to the frequency to sample the data input (column 7 line 60 to column 8 line 17) thus triggering the operation in changing in flow of figure 5], since the synchronization circuit is arranged to operate as such, it is inherent that it contains an adaptable timer circuit.

12. As per claim 6:

Hao disclosed a data processing apparatus according to claim 5, wherein the synchronization circuit inherently has the adaptable timer circuit (see rejection of claim 5), and the circuit is arranged to measure a duration of a synchronization interval in the communication signal preceding bits (start bits) that contribute to the data word [measure the duration of the start bit to determine the baud rate (column 7 line 60 to column 8 line 17)], and to set the frequency that will be used to trigger execution of the series of instructions dependent on the measured duration [the synchronization circuit is adapt to the frequency to sample the data input (column 7 line 60 to column 8 line 17) thus triggering the operation in changing in flow of figure 5].

13. As per claim 7:

Hao disclosed a data processing apparatus according to claim 6, wherein the timer circuit is arranged to detect presence or absence of a validation part (start bits) in the communication signal prior to bits that contribute to the data word (start bit is not part of the character received), the timer circuit generating execution trigger signals only upon detection of the presence of the validation part [timer circuit would not calculate value of M and BT till the detection of start bits thus would not enable the synchronization circuit to further trigger operation in the flow of figure 5 (column 7 lines 47-64)].

14. As per claim 8:

Hao disclosed a data processing apparatus according to claim 1, wherein the processor circuit (element 12 figure 4, The operand length, is not patentably distinct as it is possible that the operand length of the instruction executed by the processor in the prior art could be changed and there would be no difference in performance over the processor of the prior art. See MPEP 2144.04 section IV).

15. As per claim 9:

The additional limitation(s) of claim 9 basically recite the additional limitation(s) of claim 1. Therefore, claim 9 is rejected for the same reason(s) as claim 1.

Maintained Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hongbin Hao et al. (U.S. 6,163,586), further in view of Wishneusky et al. (U.S. 4,975,828).

18. As per claim 3:

Hao disclosed a data processing apparatus according to claim 2.

Hao failed to teach said cumulative information comprises one or more parity bits.

However, Wishneusky disclosed a data processing apparatus (figure 2) that support the calculation of parity in a cumulative bit by bit fashion (column 27 lines 21-25, column 29 lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the cumulative calculation parity instruction into the series to series of instructions to calculate parity as part of the cumulative information in the apparatus of Hao because Wishneusky teaches that inclusion of such instruction can help the apparatus performance in time critical task associated with receiving and sending of data word (Wishneusky column 6 lines 28-32). Including the cumulative calculation of parity further enhances the speed of the method of baud rate detection and character configuration in Hao by speeding up the process of assembling the incoming predetermined characters (AT or at) (Hao column 1 lines 59-64).

Response to Arguments

19. The arguments presented by Applicant in the response, received on 7/23/2007 are not considered persuasive.

20. Applicant argues "Hao discloses a "programmable processor circuit," microprocessor core 22. However, the microprocessor core of Hao is not believed to execute a plurality of series of programmed instructions in support of receiving or outputting, each time a reception of a respective one of the temporally successive bits, the processor circuit "

This argument is not found to be persuasive for the following reason. The examiner first notes that element 20 is cited as the programmable processor circuit. Figure 5 shows a hardwired state diagram of element 20 within figure 4. This element is programmable, since it's originally programmed prior to fabrication of the overall element 20. An instruction in its broadest sense is a command and/or explanation of how to perform a given task. In this definition, instructions are present within the state diagram to perform comparison to detect certain given characters at elements 58, 68, 70, and 80. These comparisons make up the series of programmed instructions and are done in support of receiving and outputting characters for input/output elements 14 and 16. Thus, Hao correctly reads upon the claimed limitation.

21. Applicant argues "Hao failed to teach a synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective ones of the temporally successive bits."

This argument is not found to be persuasive for the following reason. Element 32 performs the determining steps of elements 56 and 64, which determines is a start bit is within a legal window. If a start bit is within a legal window, this triggers the state diagram to continue to elements such as 58, 68, 70, and 80 that perform a series of instructions. Thus, Hao correctly reads upon the claimed limitation.

Conclusion

THIS ACTION IS MADE FINAL.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

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